Total Power Conversion Solutions for Computer Motherboards Using HIP6017, HIP6019 Controller ICs

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Introduction

Keeping pace with today's high-performance desktop PC architectures, the HIP6017 and HIP6019 controller/regulator ICs respond to the need for increased integration and reduced system-level costs. The Intersil HIP6017 and HIP6019 are complex controllers that integrate one and two, respectively, switching regulators, a linear controller, and a linear regulator in a single 28-lead SOIC package. The switching converters employ voltage-mode control architecture and high circuit performance is insured by the use of high Gain - Bandwidth Product (GBWP) error amplifiers, high-accuracy references, a programmable free-running oscillator, and adaptable shoot-through protection. The ICs offer a full range of protection features including over-current, over-voltage, as well as fault condition signaling and shutdown. All these combined features make the HIP6017 and HIP6019 ideal as total microprocessor point-of-use power supply solution providers [1, 2]. Figure 1 presents a simple block diagram of the HIP6017/HIP6019 application circuit.

The evaluation board features a 5-bit DAC-controlled synchronous buck converter targeted at the microprocessor core voltage, an adjustable standard buck converter (HIP6019EVAL1 only) supplying the I/O circuitry, an adjustable linear controller aimed at the GTL bus, and an adjustable linear regulator with built-in pass element to provide power to the clock generator. The HIP6017 is ideally suited for PC applications employing an ATX power supply, while the HIP6019 addresses the same need in PCs using a PS2 power supply or in situations where the 3.3V output of the ATX supply does not provide adequate regulation or transient response. Table 1 summarizes the target design parameters of the four on-board regulator blocks (three in case of HIP6017EVAL1).

The four core regulator reference designs presented in Table 2 share much common circuitry and the same printed circuit board. They highlight the operation of the HIP6017/HIP6019 controllers in an embedded motherboard application environment and the difference amongst paired designs resides in the step load capability for given output regulation limits (see Table 1 for such regulation limit examples). While design examples 1 and 2 conform to the stringent requirements of Intel's converter design guidelines, design examples 1A and 2A account for the practical experience of PC system designers. In contrast to the conservative worst-case specifications published by Intel, practical experience of PC system designers reveals microprocessor core currents 30% lower than the theoretical absolute maximum levels. This experience reflects in the design of the core regulator, as shown in examples 1A and 2A. The design engineer is encouraged to modify the board according to his own experience or specifications, and the evaluation platform is laid out to accommodate this. The core regulator of HIP6017/HIP6019EVAL1 ships populated as design example 1A.

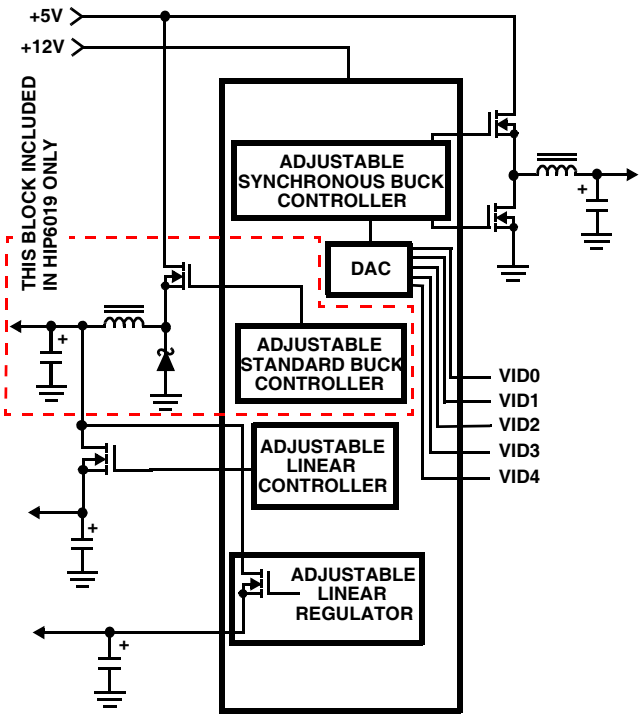


FIGURE 1. HIP6017/HIP6019 EVAL1 BLOCK DIAGRAM

Quick Start Evaluation

The inputs of both evaluation platforms will accept either standard power supplies or an ATX-style power supply. The outputs can be exercised using either resistive loads, electronic loads, or the Intel Slot 1 EMT tool. Shielded scope probe test points on the dynamic outputs (core, I/O, and GTL bus) allow for accurate inspection of the output power quality. Before proceeding, please consult Table 1 for the evaluation board's design envelope characteristics.

TABLE 1. HIP6017/HIP6019EVAL1 DESIGN PARAMETERS

OUTPUT	NOMINAL VOLTAGE (V)	STATIC TOLERANCE (±,%)	DYNAMIC TOLERANCE (±,%)	NOMINAL CURRENT (A)	MAXIMUM CURRENT (A)	MAXIMUM CURRENT STEP (A)	MAXIMUM SLEW RATE (A/µs)
VCC_CORE	2.8	2.14	4.28	10	14.2	9.5	30
VCC_L2	3.3	5.0	5.0	5	8	7	1
VCC_VTT	1.5	9.0	9.0	1	4	3	8
VCC_CLK	2.5	4	4	0.1	0.2	N/A	N/A

TABLE 2. HIP6017/HIP6019EVAL1 CORE REGULATOR DESIGN EXAMPLES

COMPONENT DESCRIPTION	REF. DES.	EXAMPLE 1 V_{OUT} = 2.8V I_{OUT} = 14.2A I_{OUT_STEP} = 13.5A	EXAMPLE 1A V_{OUT} = 2.8V I_{OUT} = 14.2A I_{OUT_STEP} = 9.5A	EXAMPLE 2 V_{OUT} = 2.0V I_{OUT} = 16.0A I_{OUT_STEP} = 15.6A	EXAMPLE 2A V_{OUT} = 2.0V I_{OUT} = 16.0A I_{OUT_STEP} = 11.0A
MOSFETs	Q1 Q2	HUF76139 HUF76139	HUF76139 HUF76139	HUF76143 HUF76143	HUF76143 HUF76143
OCSET RESISTOR	R2	1.3kΩ	1.3kΩ	1.1kΩ	1.1kΩ
OUTPUT INDUCTOR	L3	2.9µH (9T of 16AWG on T60-52 core)	2.9µH (9T of 16AWG on T60-52 core)	2.2µH (7T of 16AWG on T68-52A core)	2.2µH (7T of 16AWG on T68-52A core)
INPUT CAPACITORS	C1-13	4 (EEUFA1A10)	4 (EEUFA1A10)	9 (EEUFA1A10)	8 (EEUFA1A10)
OUTPUT CAPACITORS	C24-36	9 (EEUFA1A10)	7 (EEUFA1A10)	11 (EEUFA1A10)	8 (EEUFA1A10)
OFFSET RESISTOR	R9	732kΩ	732kΩ	432kΩ	432kΩ

On either board, if using an Intel Slot 1 EMT Tool, the core regulator VID jumpers located on the evaluation board are in parallel with the ones located on the tool itself, so remember to de-populate one set of jumpers completely and use the other set to dial-in the desired output voltage.

HIP6017EVAL1

The easiest way to power this board is by using an ATX-type computer power supply. Simply plug the appropriate supply connector into the on-board receptacle (J2), connect the outputs (VCC_CLK, VCC_CORE, and VCC_VTT) to the desired loads, and power-up the board.

If using standard laboratory power supplies, make sure the power-up sequence follows this order: 3.3V supply, followed by the 5V and 12V supplies in no particular order. This sequence is required by the IC's sophisticated monitoring and protection circuitry.

HIP6019EVAL1

Similarly, the easiest way to power this board is also by using an ATX-type PC power supply. Plug the appropriate output connector into the evaluation board's input receptacle (J2), connect the desired output loads, and power-up. If using standard laboratory equipment, the input supplies (5V and 12V) do not require any special sequencing.

HIP6017/HIP6019EVAL1 Reference

The evaluation board is designed to simultaneously meet all the applicable criteria outlined in Table 1 (HIP6017EVAL1 does not provide the 3.3V I/O voltage). The following section highlights some of the most important features of this system's power solution.

ATX Power Supply Control Interface

JP5 allows control of the power supply. By placing the jumper in the 1-2 position, the $\overline{\text{PS-ON}}$ (output enable) input of the ATX supply is connected to ground, thus unconditionally enabling the outputs. Placing the jumper in the 2-3 position connects the supply control pin to the drain of Q5 (see Figure 2). When ATX supply is turned on, the 5V stand-by output turns Q5 on and enables the power supply outputs. If FAULT/RT pin goes high, Q6 latches on, thus turning off Q5 and disabling the power supply outputs. Cycling power off and then back on re-enables the power supply. The sole purpose of this circuit is to exemplify a possible interface between the control circuit's FAULT output and an ATX power supply. In case of an over-voltage event, this circuit disables the input supply much faster than its internal short-circuit protection, thus minimizing any risks of power supply failure.

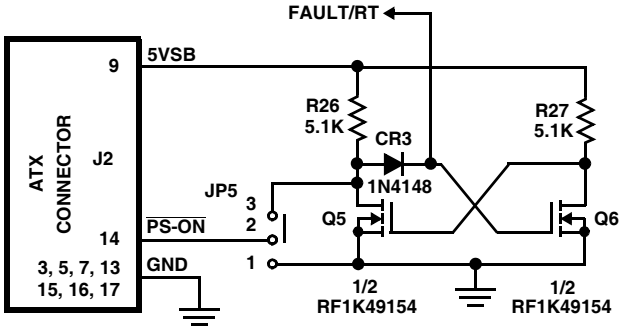


FIGURE 2. ATX POWER SUPPLY CONTROL CIRCUIT

Lossless Output Voltage Droop with Load

The switching regulators on the HIP6017/HIP6019EVAL1 boards implement output voltage droop functions, where the output voltage sags proportionately with the output current. Although not necessary for proper circuit operation, this method takes advantage of the static regulation limits to improve the dynamic regulation by expanding the available headroom for transient edge output excursion. In such practical applications, compared to a non-droop implementation, this translates to fewer output capacitors or better regulation for the same type and number of capacitors. Figure 3 details the output voltage characteristics of a converter with 2.3% droop compared to a non-droop implementation.

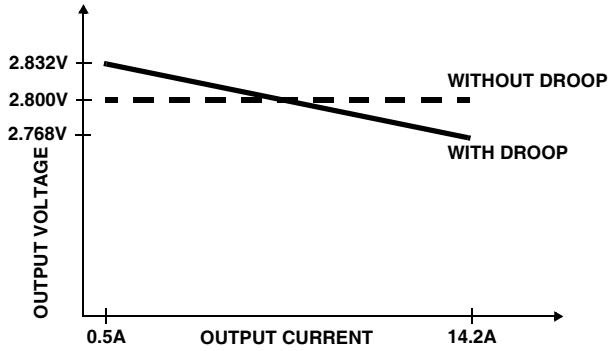


FIGURE 3. OUTPUT VOLTAGE DROOP AT 2.8V DAC SETTING

In contrast to droop implementation involving a resistive element placed in the output current path, this method does not involve the additional power loss introduced by the resistor. By moving the voltage regulation point ahead of the output inductor (at the PHASE node), droop becomes equal to the average voltage drop across the output inductor's DC resistance as well as any distributed resistance. To insure symmetric output voltage excursions about the set voltage in response to load transients, the output voltage is offset above the nominal level by half the calculated droop.

Over-Current Protection

The switching regulators within HIP6017 and HIP6019 employ a lossless current sensing technique based on the upper MOSFET's $r_{DS(ON)}$. During the ON-time of the upper MOSFET, its drain-to-source voltage is compared with a user-adjustable voltage created by an internal current source across R_{OCSET} (i.e., R1, R2 in the schematic). When the MOSFET's drain-to-source voltage exceeds the preset threshold, the regulator immediately shuts down all outputs and initiates a soft-start cycle. If the condition persists, the third shutdown latches the chip off. Cycling the bias voltage OFF and ON resets the protection circuitry.

The linear regulator outputs employ a different method of over-current detection. Given the relatively large $r_{DS(ON)}$ of the pass devices, a short-circuit condition usually translates into a dip in the output voltage. If the output voltage (as sensed at the feedback pin) dips below approximately 75% of the set point, this undervoltage is interpreted as an over-current event and the control IC reacts accordingly, shutting down all outputs and cycling the soft-start.

The internal regulator is protected by an additional internal output current mirror. Output current exceeding the preset threshold (see data sheet) generates a similar response. Any over-current event on any output is reported by the toggle of the PGOOD output.

Over-Voltage Protection

Both switching regulator outputs are protected against over-voltage events. The VCC_L2 regulator (standard buck, HIP6019EVAL1 only) has a threshold internally set at 4.3V. The microprocessor core regulator (synchronous buck) has a voltage-tracking over-voltage threshold set at 115% (typically) of the DAC setting. In case of an over-voltage event, the microprocessor core regulator attempts to regulate the output voltage at the over-voltage threshold. Both switching regulators report the overvoltage condition through a high output on the FAULT/RT pin.

In addition to the normal over-voltage operation, the microprocessor core regulator has another very useful protection feature presented in Figures 4 and 5. In case of a power-up sequence with a shorted upper MOSFET, and bias voltage above 4V (typically), an independent functional block acts upon the lower gate driver, regulating the core voltage to around 1.3V until the controller bias voltage reaches power-on threshold, at which point normal operation resumes, core voltage is regulated to 115% of the DAC setting (2.8V in this case), and fault condition is reported on the FAULT/RT pin.

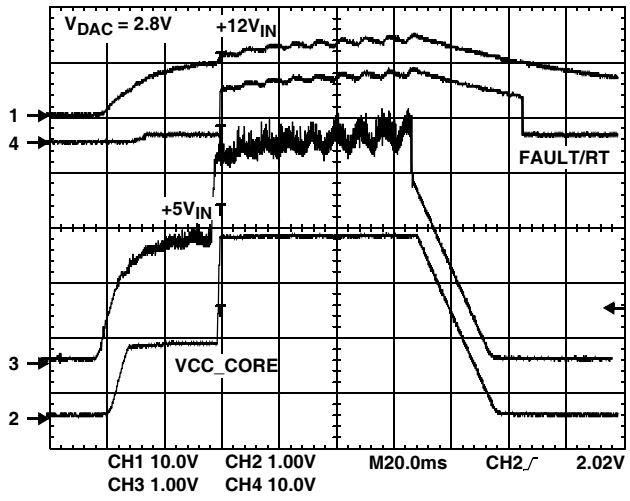


FIGURE 4. START-UP SEQUENCE WITH SHORTED Q1 (ATX CONTROL CIRCUIT BY-PASSED)

Figure 4 exemplifies operation of the evaluation board without the help of the control circuit shown in Figure 2, the ATX supply being shut down by its internal over-current protection circuitry. Proper operation of this protection feature is contingent, however, on the 12V bias voltage being sufficiently high to turn on the lower MOSFET and the lower MOSFET being a logic-level type. The circuit has been tested with several ATX supplies, and they all produced acceptable bias voltage for the operation of the protection circuitry and the on-board logic-level UltraFET™ MOSFETs.

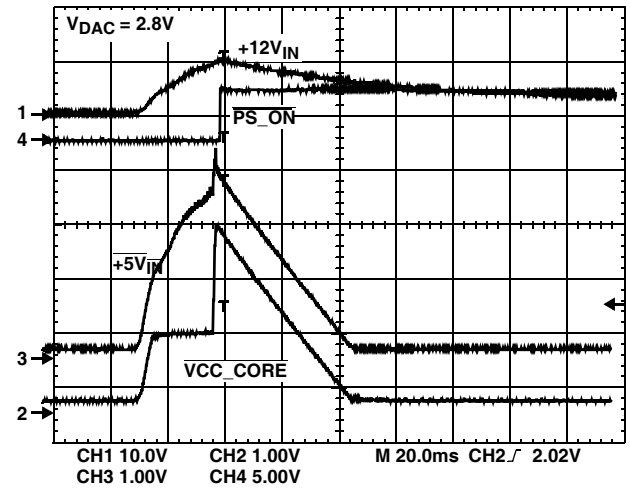


FIGURE 5. START-UP SEQUENCE WITH SHORTED Q1 (ATX CONTROL CIRCUIT ACTIVE)

Figure 5 depicts the same start-up scenario, this time with the ATX supply control interface enabled. As seen in the oscilloscope capture, as soon as power-on reset (POR) thresholds are detected, the HIP6019 detects the over-voltage condition and reports it on the FAULT/RT pin. In turn, the control circuit shuts down the ATX supply by generating a logic high at the $\overline{\text{PS-ON}}$ input.

Printed Circuit Board

The practical implementation of the circuit is done on a two-ounce, four-layer printed circuit board. The two internal layers are dedicated for ground and power planes. The layout is compact and several additional footprints are provided for increased evaluation flexibility. The component side of the board contains an embedded serpentine resistor (approx. 200mΩ) series with the drain of Q4. This resistor is not necessary for the proper operation of the circuit; its role is simply to share the power dissipation which otherwise would be dissipated entirely by Q4. Contact Intersil technical support at 1-888-INTERSIL for board layout Gerber files.

Power MOSFETs

The power transistors utilized by HIP6017/HIP6019EVAL1 belong to Intersil' newest line of 30V UltraFET MOSFETs. Featuring reduced $r_{DS(ON)}$ and low t_{rr} and Q_{rr}, these transistors allow for elimination of the traditional lower MOSFET anti-parallel schottky.

HIP6017/HIP6019EVAL1 Performance

Efficiency

Figure 6 displays the laboratory-measured efficiency of the HIP6017EVAL1 reference design versus load current, for 5V input and 100 linear feet per minute (LFM) of airflow. Due to the fact that the linear regulators efficiency is not a figure of merit for the application circuit, the efficiency results were obtained based on loading of the switching regulator output only.

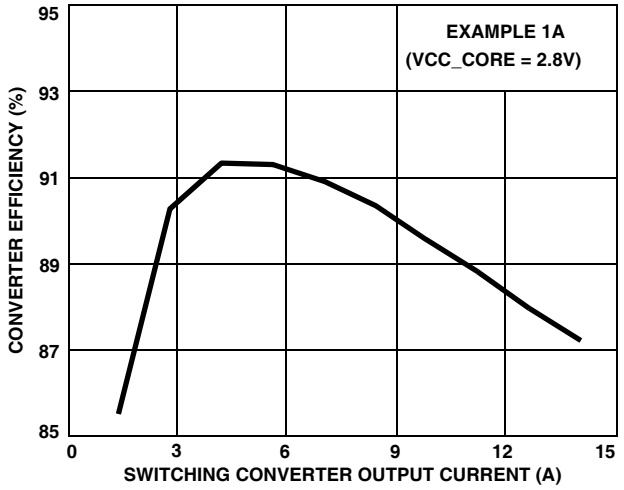


FIGURE 6. HIP6017EVAL1 MEASURED CONVERTER EFFICIENCY

Similarly, Figure 7 displays the efficiency obtained in the HIP6019EVAL1 circuit. Since this evaluation platform contains two switching regulators, both switching regulator outputs were simultaneously loaded and measured. The efficiency curve in Figure 7 represents a composite result of the overall circuit efficiency plotted against total converter output power.

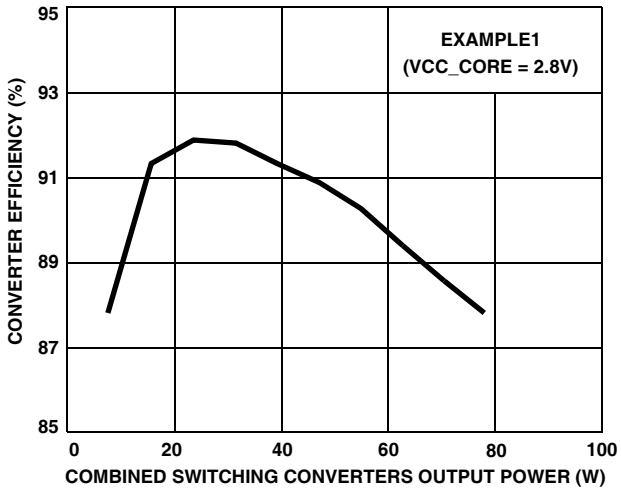


FIGURE 7. HIP6019EVAL1 MEASURED CONVERTER EFFICIENCY

Load Transient Response

Channel 4 of the oscilloscope captures presented in Figure 8 details the core voltage regulation of a HIP6019EVAL1 in response to a 12A output step load transient (larger than the 9.5A design point) as provided by an Intel Slot 1 Test Tool. All other outputs are subjected to the maximum transient loading conditions and all channels are vertically offset by the nominal output voltage settings as described in Table 1.

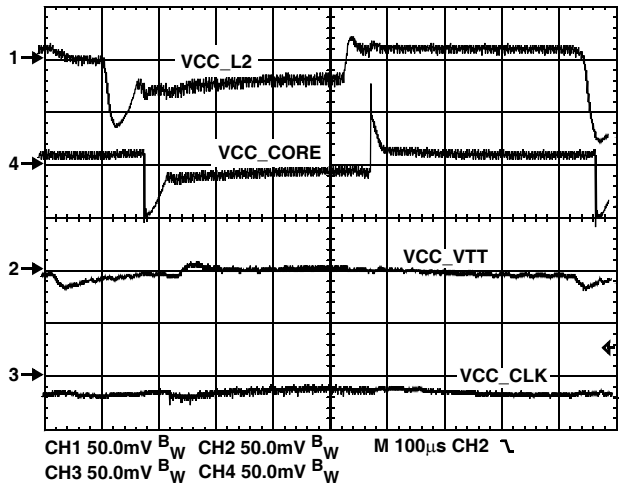


FIGURE 8. HIP6019EVAL1 OUTPUT TRANSIENT RESPONSE

HIP6017/HIP6019EVAL1 Modifications

Input Capacitors Selection

In a DC/DC converter employing an input inductor, the input RMS current is supplied entirely by the input capacitors. The number of input capacitors is usually determined by their maximum RMS current rating. The voltage rating at maximum ambient temperature of the input capacitors should be at least 1.25 to 1.5 times the maximum input voltage. High frequency decoupling (highly recommended) is implemented through the use of ceramic capacitors in parallel with the bulk aluminum capacitor filtering. The switching converter's input RMS current is dependent on the input and output voltages as well as the output current. Figure 9 shows this approximate relationships for five different levels of current. Based on the linearity of the relationship, the graph results can be interpolated for additional levels of output current. For output voltages ranging from 2 to 3V, a good approximation of the input RMS current is 1/2 the output current.

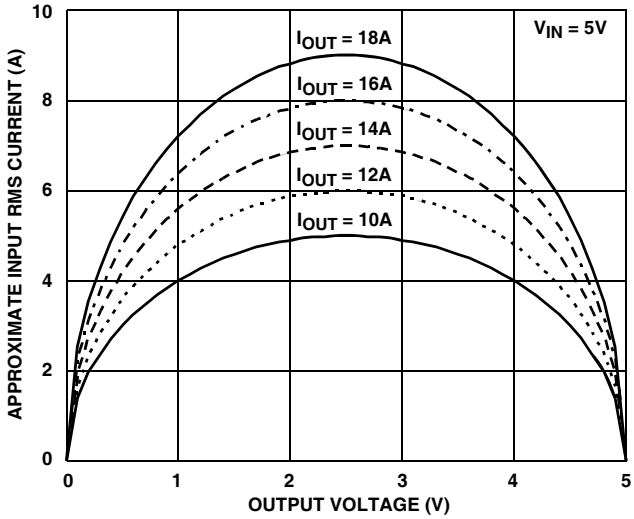


FIGURE 9. SWITCHING CONVERTER RMS INPUT CURRENT

Using the above graph and the capacitor RMS current rating, a minimum number of input capacitors can be easily determined. If the time-averaged load is different than the maximum load, the number of input capacitors may be cautiously scaled down.

Output Voltages

The synchronous buck converter supplying the microprocessor core voltage is controlled by the internal DAC. Output voltage can be adjusted by selecting the appropriate VID jumper combination. For more information please refer to the HIP6019 data sheet which contains a very comprehensive table detailing all the VID combinations and the resultant output voltages. Noteworthy is the fact the HIP6019 can be operated with or without pull-up resistors on the VID lines. If droop implementation is desired, the no-load output voltage can be determined from the following equation:

$$V_{VCC-CORE} = V_{DAC} \bullet \left(1 + \frac{R4 + R8}{R9}\right), \text{where} \quad \text{(EQ. 1)}$$

V_{DAC} = DAC-set output voltage target.

In case of the standard buck regulator, as well as the linear regulator and controller, output voltage adjustment is based

on the chip's internal bandgap voltage reference. Simple resistor value changes allow for outputs as low as 2.7V or as high as 4.2V. The steady-state DC output voltages can be set using the following equations:

For the standard buck regulator:

$$V_{VCC-L2} = V_{REF} \bullet \left(1 + \frac{R3 + R5}{R6}\right) \quad \text{(EQ. 2)}$$

For the linear controller:

$$V_{VCC-VTT} = V_{REF} \bullet \left(1 + \frac{R11}{R12}\right) \quad \text{(EQ. 3)}$$

for the linear regulator:

$$V_{VCC-CLK} = V_{REF} \bullet \left(1 + \frac{R13}{R14}\right), \text{where} \quad \text{(EQ. 4)}$$

V_{REF} = HIP6019 internal reference voltage (typically 1.265V).

Note the fact that since the internal regulator draws its input power from the FB2 pin, V_{VCC_CLK} cannot exceed the voltage set by the user for the V_{VCC_L2} output. Similarly, V_{VCC_VTT} cannot be set higher than its input source (V_{VCC_L2} in HIP6019EVAL1, and +3.3V in HIP6017EVAL1.)

Output Capacitors Selection

Selection of the output capacitors should take into account all the component parasitics. Table 2 offers some recommendations for the core regulator based on the output requirements.

Sizing the output capacitor for the internal linear regulator is a somewhat different procedure, mainly due to the fact that the stability of this regulator depends on the characteristics of this output capacitor. The output capacitance and ESR determine the loop stability, and Figure 10 helps quantify the tradeoff between the type of capacitor used and the resulting regulator loop phase margin. As with any other design, the selection should be made in such a way as to provide a minimum of 45 degrees of phase margin (selection should be made above the dotted line). Additionally, the selected output capacitor should be able to keep the output voltage within desired regulation limits when subjected to typical load transients.

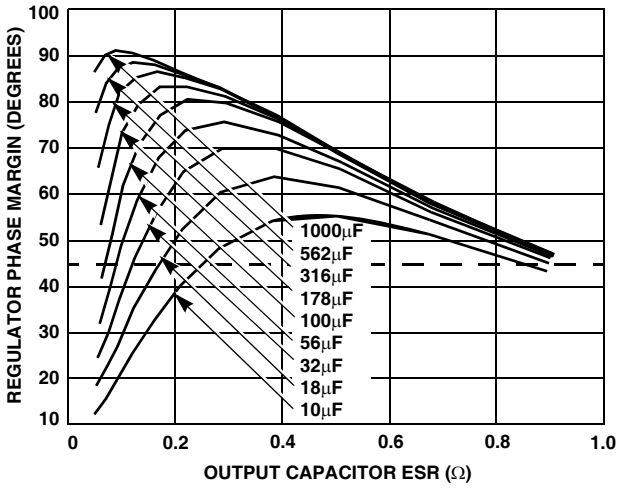


FIGURE 10. VCC_CLK REGULATOR LOOP PHASE MARGIN vs OUTPUT CAPACITOR CHARACTERISTICS

Conclusion

The HIP6019EVAL1 board lends itself to a wide variety of high-power DC-DC microprocessor converter designs. The built-in flexibility allows the designer to quickly modify for applications with various requirements, the printed circuit board being laid out to accommodate the necessary components for operation at currents up to 19A.

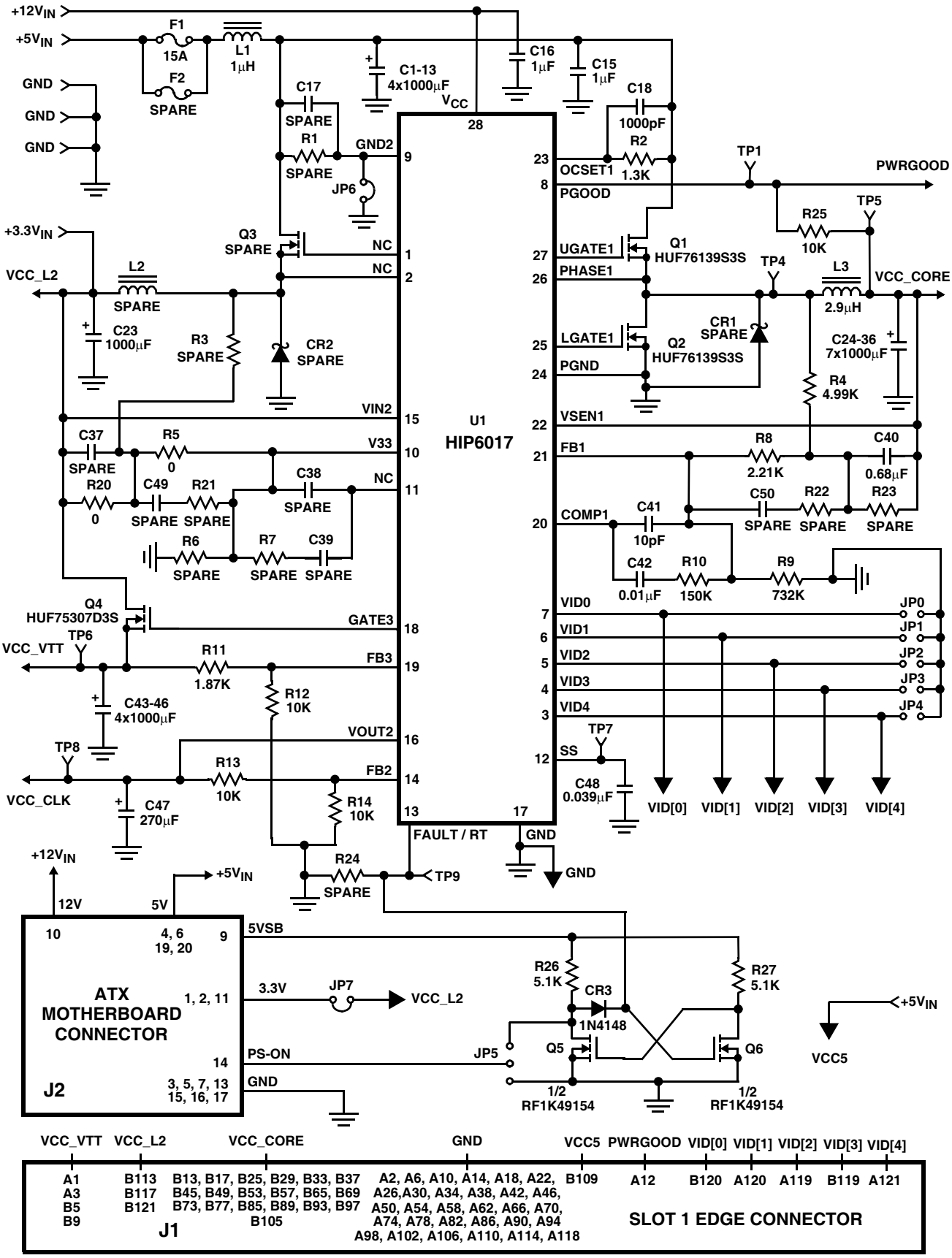
References

For Intersil documents available on the internet, see web site http://www.intersil.com.

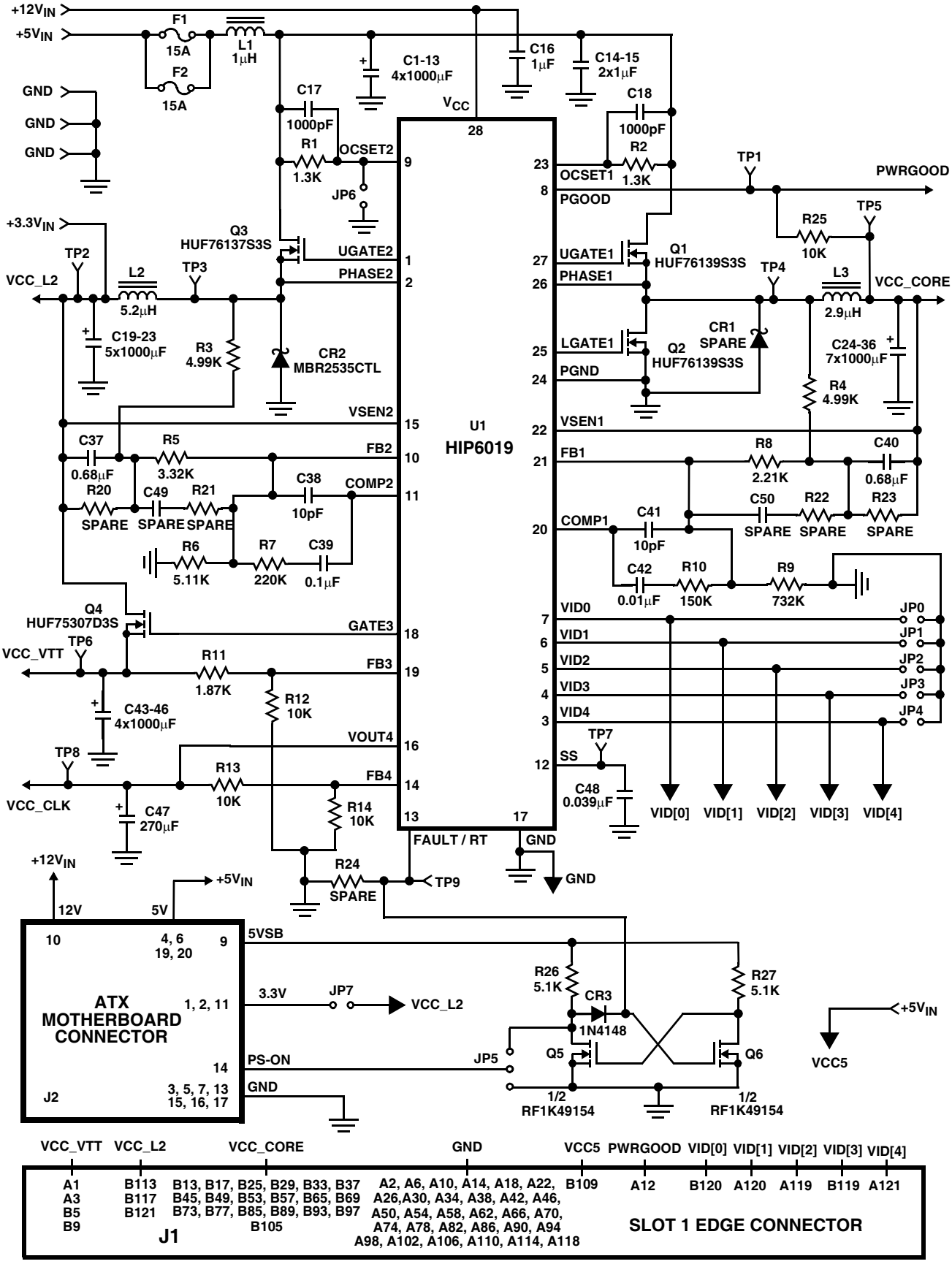
[1] *HIP6019 Data Sheet*, Intersil Corporation, FN4490.

[2] *HIP6017 Data Sheet*, Intersil Corporation, FN4496.

HIP6017EVAL1 Schematic



HIP6019EVAL1 Schematic



Bill of Materials for HIP6017EVAL1

REF	PART #	DESCRIPTION	PACKAGE	QTY	VENDOR
C1-4, 23, 28-34, 43-46	EEUFA1A10	Aluminum Capacitor, 10V, 1000µF	Radial 8x20	16	Panasonic
C5-13, 19-22, 24-27, 35, 36	Spare	Aluminum Capacitor	Radial 8x20		
C14	Spare	Ceramic Capacitor	1206		
C15, 16	1206YZ105MAT1A	Ceramic Capacitor, X7S, 16V, 1.0µF	1206	3	AVX
C17, 37-39, 49, 50	Spare	Ceramic Capacitor	0805		
C18	1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	1	Various
C40	0.68µF Ceramic	Ceramic Capacitor, X7R, 16V	1206	1	AVX
C41	10pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	1	Various
C42	0.01µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
C47	6MV270GX	Aluminum Capacitor, 6.3V, 270µF	Radial 6.3x11	1	Sanyo
C48	0.039µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
CR1	Spare	Schottky Rectifier	DO215AB		
CR2	Spare	Schottky Rectifier	D^2-PAK		
CR3	1N4148	Silicon Rectifier, 100mA, 75V	DO35	1	Motorola
F1	251015A	Miniature Fuse, 15A	Axial	1	Littelfuse
J1	71796-0005 145251-1	Slot 1 Edge Connector		1	Molex AMP
J2	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		1	Molex
JP6, R5, 20	0Ω	Shorting Resistor	0805	3	Various
JP7	16AWG	Jumper, Ni-plated Copper Conductor			
L1	PO720	1µH Inductor, 7T of 16AWG on T50-52 Core	Wound Toroid 18x18x9	1	Pulse
L2	Spare	Inductor	Wound Toroid 20x20x10		
L3	PO716	2.9µH Inductor, 9T of 16AWG on T60-52 Core	Wound Toroid 20x20x10	1	Pulse
Q1, Q2	HUF76139S3S	UltraFET™ MOSFET, 30V, 7.5mΩ	TO-263	2	Intersil
Q3	Spare	MOSFET	TO-263		
Q4	HUF75307D3S	UltraFET™ MOSFET, 55V, 90mΩ	TO-252	1	Intersil
Q5, 6	RF1K49154	MegaFET MOSFET, 60V, $V_{GS(MIN)}$ = 2V, 130mΩ	SO-8	1	Intersil
R1, 3, 6, 7, 21-24	Spare	Resistor	0805		
R2	1.3kΩ	Resistor, 5%, 0.1W	0805	1	Various
R4	4.99kΩ	Resistor, 1%, 0.1W	0805	1	Various
R8	2.21kΩ	Resistor, 1%, 0.1W	0805	1	Various
R9	732kΩ	Resistor, 1%, 0.1W	0805	1	Various
R10	150kΩ	Resistor, 5%, 0.1W	0805	1	Various
R11	1.87kΩ	Resistor, 1%, 0.1W	0805	1	Various
R12-14, 25	10kΩ	Resistor, 1%, 0.1W	0805	4	Various
R26, 27	5.1kΩ	Resistor, 5%, 0.1W	0805	2	Various

Bill of Materials for HIP6017EVAL1 (Continued)

REF	PART #	DESCRIPTION	PACKAGE	QTY	VENDOR
$+5V_{IN}$, $+12V_{IN}$, $+3.3V_{IN}$, GND, VCC_CORE, VCC_CLK, VCC_L2, VCC_VTT	1514-2	Terminal Post		14	Keystone
TP1,4, 7-9	SPCJ-123-01	Test Point		6	Jolo
TP3	Spare	Test Point			
TP2,5,6	1314353-00	Test Point, Scope Probe		3	Tektronics
U1	HIP6017CB	Dual PWM and Dual Linear Controller	SOIC-28	1	Intersil

Bill of Materials for HIP6019EVAL1

REF	PART #	DESCRIPTION	PACKAGE	QTY	VENDOR
C1-4, 19-23, 28-34, 43-46	EEUFA1A102	Aluminum Capacitor, 10V, 1000µF	Radial 8x20	20	Panasonic
C5-13, 24-27, 35, 36	Spare	Aluminum Capacitor	Radial 8x20		
C14-16	1206YZ105MAT1A	Ceramic Capacitor, X7S, 16V, 1.0µF	1206	3	AVX
C17-18	1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	2	Various
C37, C40	0.68µF Ceramic	Ceramic Capacitor, X7R, 16V	1206	2	AVX
C38, 41	10pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	2	Various
C39	0.1µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
C42	0.01µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
C47	6MV270GX	Aluminum Capacitor, 6.3V, 270µF	Radial 6.3x11	1	Sanyo
C48	0.039µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
C49-50	Spare	Ceramic Capacitor	0805		
CR1	Spare	Schottky Rectifier	DO215AB		
CR2	MBR2535CTL	Schottky Rectifier, 25A, 35V	D^2-PAK	1	Motorola
CR3	1N4148	Silicon Rectifier, 100mA, 75V	DO35	1	Motorola
F1, 2	251015A	Miniature Fuse, 15A	Axial	2	Littelfuse
J1	71796-0005 145251-1	Slot 1 Edge Connector		1	Molex AMP
J2	39-29-9203	20-pin Mini-Fit, Jr. Header Connector		1	Molex
JP6, 7	Spare	Jumper			
L1	PO720	1µH Inductor, 7T of 16AWG on T50-52 Core	Wound Toroid 18x18x9	1	Pulse
L2	PO743	5.2µH Inductor, 13T of 16AWG on T60-52 Core	Wound Toroid 20x20x10	1	Pulse
L3	PO716	2.9µH Inductor, 9T of 16AWG on T60-52 Core	Wound Toroid 20x20x10	1	Pulse
Q1, Q2	HUF76139S3S	UltraFET MOSFET, 30V, 7.5mΩ	TO-263	2	Intersil
Q3	HUF76137S3S	UltraFET MOSFET, 30V, 9mΩ	TO-263	1	Intersil
Q4	HUF75307D3S	UltraFET MOSFET, 55V, 90mΩ	TO-252	1	Intersil
Q5, 6	RF1K49154	MegaFET MOSFET, 60V, $V_{GS(MIN)}$ = 2V, 130mΩ	SO-8	1	Intersil

Bill of Materials for HIP6019EVAL1 (Continued)

REF	PART #	DESCRIPTION	PACKAGE	QTY	VENDOR
R1, 2	1.3kΩ	Resistor, 5%, 0.1W	0805	2	Various
R3, 4	4.99kΩ	Resistor, 1%, 0.1W	0805	2	Various
R5	3.32kΩ	Resistor, 1%, 0.1W	0805	1	Various
R6	5.11kΩ	Resistor, 1%, 0.1W	0805	1	Various
R7	220kΩ	Resistor, 5%, 0.1W	0805	1	Various
R8	2.21kΩ	Resistor, 1%, 0.1W	0805	1	Various
R9	732kΩ	Resistor, 1%, 0.1W	0805	1	Various
R10	150kΩ	Resistor, 5%, 0.1W	0805	1	Various
R11	1.87kΩ	Resistor, 1%, 0.1W	0805	1	Various
R12-14, 25	10kΩ	Resistor, 1%, 0.1W	0805	4	Various
R20-24	Spare	Resistor	0805		
R26, 27	5.1kΩ	Resistor, 5%, 0.1W	0805	2	Various
$+5V_{IN}$, $+12V_{IN}$, GND, VCC_CORE, VCC_CLK, VCC_L2, VCC_VTT	1514-2	Terminal Post		12	Keystone
TP1, 3, 4, 7-9	SPCJ-123-01	Test Point		6	Jolo
TP2, 5, 6	1314353-00	Test Point, Scope Probe		3	Tektronics
U1	HIP6019CB	Dual PWM and Dual Linear Controller	SOIC-28	1	Intersil